

WHAT IS CLAIMED IS:

1. A method of manufacturing semiconductor devices,
comprising the steps of:

5 forming a plurality of gates on a semiconductor substrate;

forming an insulation layer on an entire surface of the
semiconductor substrate to coat the plurality of gates;

10 selectively removing the insulation layer by using a first
mask pattern to form a contact hole, which exposes a source/drain
junction and a conductive layer in a portion of the gates in the
semiconductor substrate;

15 removing the first mask pattern and forming a second mask
pattern on the selectively removed insulation layer, the second
mask pattern exposing the p+ source/drain junction in the
semiconductor substrate;

implanting ion into the p+ source/drain junction in the
semiconductor substrate by using the second mask pattern as a
mask;

20 removing the second mask pattern and rapid thermal annealing
the entire substrate in a activation temperature range of dopant
which is implanted in the ion implantation step; and

burying the contact hole with conductive material to form
a bit line contact plug.

2. The method of manufacturing semiconductor devices according to claim 1, wherein the ion implantation step is performed with the dose of $4.5\sim6\times10^{15}$ atoms/cm².

5 3. The method of manufacturing semiconductor devices according to claim 1, wherein the ion implantation step is performed with the energy of 10~24keV.

10 4. The method of manufacturing semiconductor devices according to claim 1, wherein a tilt angle is adjusted in a range of about 0 to 60 degrees in the ion implantation step.

15 5. The method of manufacturing semiconductor devices according to claim 1, wherein an orientation is adjusted in a range of about 0 to 90 degrees in the ion implantation step.

6. The method of manufacturing semiconductor devices according to claim 1, wherein rotation is adjusted within four times in the ion implantation step.

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7. The method of manufacturing semiconductor devices according to claim 1, wherein the rapid thermal annealing is performed at a temperature of 830°C or less.

8. The method of manufacturing semiconductor devices according to claim 7, wherein the rapid thermal annealing uses 1 to 25slm N₂ gas as purge gas.

5 9. The method of manufacturing semiconductor devices according to claim 7, wherein the rapid thermal annealing is performed at a heating rate of about 10 to 100°C/sec.